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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,452	09/10/2003	Thane M. Larson	10008321-2	4904
7590	09/21/2005			
HEWLETT-PACKARD COMPANY				EXAMINER
Intellectual Property Administration				DINH, TUAN T
P.O. Box 272400				ART UNIT
Fort Collins, CO 80527-2400				PAPER NUMBER
				2841

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/659,452	LARSON, THANE M.
	Examiner Tuan T. Dinh	Art Unit 2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 01 July 2005.  
 2a) This action is FINAL.                            2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 13-20 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 13-20 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>09/10/03</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

**DETAILED ACTION**

***Election/Restrictions***

1. Applicant's election without traverse of Group II (claims 13-20) in the reply filed on 07/01/05 is acknowledged.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 13, 16, 18-20 rejected under 35 U.S.C. 102(b) as being anticipated by Jodoin (U.S. Patent 4,636,918) submitted by applicant.

As to claims 13, 16, Jodoin discloses an assembled substrate, which is a PCB, as shown in figures 5-6 comprising:

a substrate (14, column 4, line 44) having first and second sides (top and bottom surfaces), and

first and second electrical contact areas (PTH-16 and conductors 18) on said first and second sides;

an electrical component (10) having a plurality of leads (12) electrically connected to said first electrical contact area of said substrate (14); and  
a capacitor plate (20, column 4, line 49) electrically connected to said second electrical contact area on said second side of said substrate (14) substantially opposite said first electrical contact area of said substrate.

As to claim 18, Jodoin discloses said capacitor plate (20) having a plurality of layers of dielectric material (30-figure 6) separating a plurality layers of conductive material (24, 26), see column 4, lines 7-9.

As to claim 19, Jodoin discloses said capacitor plate (20) comprises: a plurality of conductive power and ground planes (24, 26), wherein said plurality of conductive power and ground planes are separated by one or more dielectric layers (30) including a dielectric layer chosen from a ceramic.

As to claim 20, Jodoin discloses said capacitor plate (20) is attached by solder to said second electrical contact area on said second side of said substrate (14) (it is inherently to feed the pins/leads of the capacitor plate into PTH (16) by applying solder for electrical connection).

4. Claims 13, 16-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kozak et al. (U.S. Patent 6,414,850) submitted by applicant.

As to claims 13, 16-17, Kozak et al. discloses an assembled substrate, which is a PCB, as shown in figures 1-7 comprising:

a substrate (114) having first and second sides (top and bottom surfaces), and

first and second electrical contact areas (134) on said first and second sides; an electrical component (112), which is a BGA device (column 4, line 26) having a plurality of leads (ball pads underneath of the chip 112) electrically connected to said first electrical contact area of said substrate (114); and a capacitor plate (412, column 4, lines 33-34) electrically connected to said second electrical contact area on said second side of said substrate (114) substantially opposite said first electrical contact area of said substrate.

As to claim 18, Kozak et al. discloses said capacitor plate (412) having a plurality of layers of dielectric material (618a-e-figure 6) separating a plurality layers of conductive material (612a-c and 614a-c, see figure 6), see column 4, lines 55-59.

As to claim 19, Kozak discloses said capacitor plate (412) comprises: a plurality of conductive power and ground planes (614, 612), wherein said plurality of conductive power and ground planes are separated by one or more dielectric layers (618) including a dielectric layer chosen from a ceramic.

As to claim 20, Kozak discloses said capacitor plate (412) is attached by solder to said second electrical contact area on said second side of said substrate (114).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozak et al. ('850) or Jodoin ('918) in view of Kabadi (U.S. Patent 6,097,609), and further in view of Wisser (U.S. patent 3,721,941).

As to claim 14, Kozak or Jodoin disclose all of the limitations of the claimed invention, except for a first interposer (or socket) between said component and said first electrical contact area on said first side of said substrate; and a second interposer (or socket) between said capacitor plate and said second electrical contact area on said second side of said substrate.

Kabadi teaches a dual socket for two components (320, 360-figure 4), and further Wisser shows a multiple socket with pins feeding through a PCB (21, see figures 1-2).

Therefore, It would have been obvious to one having ordinary skill in the art at the time the invention was made to have teaching of Kabadi and Wisser employ in the substrate of Kozak et al. or Jodoin in order to perform interconnections between components on board without any manner damage.

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Douglass, Frankeny et al., and Norskov disclose related art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tuan Dinh  
September 15, 2005.